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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/753,103	CHEN ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *14 and 23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of the Group I invention (claims 1-13 and 15-22) (NAND flash memory cell array) in the reply filed on 5/18/05 is acknowledged.

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement filed 4/12/04. A signed copy of Form PTO-1449 is enclosed with this office action.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "source diffusion in the active area directly beneath the select gate at a second end of each row" is not shown in the Drawings and must be shown or the feature canceled from the claims. In particular, gate stacks 37/38 are seen to laterally surround the source diffusion area. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. ***Claim 1 and claims 2-13 dependent on claim 1*** are objected to because of the following informalities: the wording "a plurality of vertically stacked pairs" (claim 1, line 2) should be replaced by: "a plurality of stacked gates consisting of vertically stacked pairs". Appropriate correction is required.

4. ***Claim 15 and claims 16-18 dependent on claim 15*** are objected to because of the following informalities: the wording "a plurality of vertically stacked pairs" (claim 15, line 2) should be replaced by: "a plurality of stacked gates consisting of vertically stacked pairs". Appropriate correction is required.

5. ***Claim 19 and claims 20-22 dependent on claim 19*** are objected to because of the following informalities: the wording "a plurality of vertically stacked pairs" (claim 19, line 2) should be replaced by: "a plurality of stacked gates consisting of vertically stacked pairs". Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. The term "relatively" in ***claim 3*** as employed in three different places, namely: in "relatively thin" (line 1), in "first relatively thick" (line 2) and in "second relatively thick" (lines 3-4) is a relative term which renders the claim indefinite. The term "relatively" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

8. The term "relatively large" in ***claim 4*** is a relative term which renders the claim indefinite. The term "relatively large" (line 3) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

9. The term "high-voltage" in ***claim 4*** is a relative term which renders the claim indefinite. The term "high-voltage" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

10. The term "high" in ***claim 5*** is a relative term which renders the claim indefinite. The term "high voltage"(lines 2-3) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

11. The term "high" in ***claim 6*** is a relative term which renders the claim indefinite. The term "high voltage"(line 3) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

12. The term "relative high" in ***claim 8*** is a relative term which renders the claim indefinite. The term "relatively high voltage" (line 2) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

13. The term "relatively low" in ***claim 9*** is a relative term which renders the claim indefinite. The term "relatively low voltage" (line 2) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

14. The term "relatively high" in ***claim 9*** is a relative term which renders the claim indefinite. The term "relatively high positive voltage" (lines 2-3, 4, 5, 6-7 and 8) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

15. The term "relatively high" in ***claim 10*** is a relative term which renders the claim indefinite. The term "relatively high negative voltage" (line 2) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and

one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

16. The term "relatively low" in ***claim 10*** is a relative term which renders the claim indefinite. The term "relatively low negative voltage" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

17. The term "relatively high" in ***claim 11*** is a relative term which renders the claim indefinite. The term "relatively high negative voltage" (line 2) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

18. The term "relatively low" in ***claim 11*** is a relative term which renders the claim indefinite. The term "relatively low negative voltage" (lines 2-3) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

19. The term "relatively high" in ***claim 12*** is a relative term which renders the claim indefinite. The term "relatively high positive voltage" (line 4) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

20. The term "relatively" in ***claim 17*** as employed in three different places, namely: in "relatively thin" (line 1), in "first relatively thick" (line 2) and in "second relatively thick" (lines 3-4) is a relative term which renders the claim indefinite. The term "relatively" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

21. The term "relatively large" in ***claim 18*** is a relative term which renders the claim indefinite. The term "relatively large" (line 3) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

22. The term "relatively" in ***claim 21*** as employed in three different places, namely: in "relatively thin" (line 1), in "first relatively thick" (line 2) and in "second relatively thick" (lines 3-4) is a relative term which renders the claim indefinite. The term "relatively" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

23. The term "high-voltage" in ***claim 22*** is a relative term which renders the claim indefinite. The term "high-voltage" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

24. ***Claims 1-13 and 15-22*** are rejected under 35 U.S.C. 102(b) as being anticipated by Noda (6,400,604 B2).

On claim 1: Noda teaches (title, abstract, Figures 3 and 4b, and col. 6, l. 26 – 62) a NAND flash memory cell array, comprising: a substrate 30 (col. 6, l. 30) having an active area 32 (col. 6, l. 30), a plurality (for the plurality see Figure 3 in which there are at least two control gate lines CGL depicted) of vertically stacked pairs of floating gates 35 and control gates 37 (see Figure 4b) arranged in rows above the active area, with the control gates being positioned above the floating gates, select gates aligned SG1, SG2,..., (col. 6, l. 46) with and positioned on both sides of each of the stacked gates (Figures 3 and 4b), a bit line (horizontal portion of 40 in Figure 4b) (col. 6, l. 54) above each row, a bit line diffusion 38 (col. 6, l. 49) in the active area toward a first end of each row (left end in Figure 4b), a bit line contact (vertical portion of 40) interconnecting the bit line in each row and the bit line diffusion 38, and a source region 38 (col. 6, l. 48-51) in the active area at least partially overlapped (by virtue of being produced by a self-aligned method: see col. 6, l. 48-51), in which the lateral diffusion that inherently causes a lateral spread of the implanted ions in both directions hence inter alia in directions leading under the select gate used as mask in the self-aligned process step) by the select gate at a second end of each row (right hand side corresponding to the opposite end from the bitline contact).

On claim 2: Noda teaches stacked gates and the stacked gates are self-aligned relative to each other (col. 6, l. 48-51).

On claim 3: The following rejection is provided subject to the rejection under 35 U.S.C. 112, second paragraph, based on the best understanding by examiner, which is that "relatively" merely is to indicate a juxtaposition of material layers thin enough for tunneling ("relatively thin") and those not necessarily thin enough for tunneling ("relatively thick"). Noda teaches including a relatively thin tunnel oxide 34 (col. 1, l. 20-35 and col. 6, l. 35-36) between the floating gates and the substrate, a first relatively thick dielectric 39 between the floating gates and the select gates, and a second relatively thick dielectric 39 between floating gates and control gates. N.B.: Attention is drawn to the appearance of a relative term, "relatively thick", and the consequent rejection under 35 U.S.C. 112, second paragraph made above. The assumption of the examiner under which the art rejection of claim 3 has been provided is that a range of thickness for both first and second "relatively thick" dielectrics that is not necessarily restricted to the regime in which tunneling can take place to an extent noticeable in the operation of the device.

On claim 4: The control gates and the select gates surround the floating gates (see Figure 4b). Referring to the rejection under 35 U.S.C., 112, second paragraph as made above, the remainder of the limitation of this claim is indefinite for containing relative terms "relatively large" and "high-voltage": some capacitance is implied by the proximity of control, floating, and select gates, and the examiner has assumed that some capacitance meets the claim in the absence within the specification of any

specific measure with which the relative terms can be viewed to acquire a definite meaning within context.

On claim 5: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted without giving weight to the limitation "high". Inherently, erase paths extend from the floating gates, through the tunnel oxide to the channel regions by virtue of the very existence of a current path for electrons between floating gate to the channel regions through FN tunneling (col. 9, l. 30-35), and high voltage is coupled to the floating gates both from the control gates and from the select gates (col. 9, l. 37-50: keep in mind the tunnel oxide does not reduce the voltage in the floating gate by any meaningful way from the voltage in the channel because it is extremely thin).

On claim 6: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted without giving weight to the limitation "high". Program paths extend from off-gate channel regions 38 between the select gates and the floating gates to the floating gates (because regions 38 are highly doped (Figure 4b) and hence substantially conductive, thereby allowing programming paths to exist); and high voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region (col. 9, l. 37-50: keep in mind the tunnel oxide does not reduce the voltage in the floating gate by any meaningful way from the voltage in the channel because it is extremely thin), said select gates being on the sides of the stacked gates toward the source diffusion region (Figures 3 and 4b).

On claim 7: Program paths extend from off-gate channel regions 38 between the select gates and the floating gates to the floating gates (because regions 38 are highly doped (Figure 4b) and hence substantially conductive, thereby allowing programming paths to exist), while the remainder of the limitation defined by claim 7 constitutes functional language: In reference to the claim language referring to said limitation, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). In the underlying case no difficulty exists in the prior art structure to impart the voltages as claimed because the select gates are independent of each other.

On claim 8: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted without giving weight to the limitation "high". The select gates in unselected cells (note that individual selection is possible; see Figures 3 and 4a,b) *can be* biased at a relatively high voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source diffusion (see for instance, col. 6, l. 63-67). Whether or not they are has no patentable weight: In reference to the claim language referring to said limitation, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it

meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). In the underlying case no difficulty exists in the prior art structure to impart the voltages as claimed because the select gates are independent of each other.

On claim 9: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted assuming that "relatively low positive voltage" and "relative high positive voltage" are terms merely indicating that the former voltage is lower than the latter voltage. The bit line for a row containing a selected cell to be programmed *can be* held at 0 volts because said bit line is conductive; a relatively low positive voltage *can be* applied to a cell select gate for the selected cell as the select gates are independent; a relatively high positive voltage *can be* applied to the source diffusion at the second end of the row in which the selected cell is located because any source region is inherently conductive; a relatively high positive voltage *can be* applied to the control gate in the selected cell; a relatively high positive voltage *can be* applied to the select gates for unselected cells, and a relatively high positive voltage *can be* applied to the control gates in the unselected cells. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 10: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted assuming that "relatively low negative voltage" and "relative high negative voltage" are terms merely indicating that the former voltage is lower in magnitude than the latter voltage. An erase path *can be* formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the bit line diffusions, the source diffusion and the P-well at 0 volts. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 11: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted assuming that "relatively low negative voltage" and "relative high negative voltage" are terms merely indicating that the former voltage is lower in magnitude than the latter voltage. An erase path *can be* formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the P-well at a positive voltage and the bit line and source diffusions floating. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the

claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 12: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted assuming that "relatively high positive voltage" merely indicates that the voltage is higher in magnitude than the zero voltage of the common source. A read path *can be* formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells (cell selection being possible in the structure defined by Figures 3 and 4a,b), with the common source at 0 volts, the bit line diffusion at 1-3 volts, and the control gate at relatively high positive voltage, and the control gate of the selected cell *can be* biased at 0-1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 13: As discussed under claim 11, an erase path *can be* formed by biasing of control gates and select gates; since this biasing can be done for each

individual member in the cell array an erase path can erase the whole cell array simultaneously; and since cells can be selected individually a program path which is single cell selectable *can be* created through appropriate biasing. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 15: Noda teaches (title, abstract, Figures 3 and 4b, and col. 6, l. 26 – 62) a NAND flash memory cell array, comprising: a substrate 30 (col. 6, l. 30) having an active area 32 (col. 6, l. 30), a plurality (for the plurality see Figure 3 in which there are at least two control gate lines CGL depicted) of vertically stacked pairs of floating gates 35 and control gates 37 (see Figure 4b) arranged in rows above the active area, with the control gates being positioned above the floating gates (see Figure 4b), select gates aligned SG1, SG2,..., (col. 6, l. 46) with and positioned on both sides of each of the stacked gates (Figures 3 and 4b), a bit line diffusion 38 (col. 6, l. 49) in the active area toward a first end of each row (left end in Figure 4b), a source diffusion 38 (col. 6, l. 48-51) in the active area directly beneath the select gate at a second end of each row (because said source diffusion at least partially overlaps the select gate as it has been created through a self-aligned process with the select gate as mask (col. 6, l. 48-51), lateral diffusion of ions implanted inherently causing a lateral spread of the implanted

ions in all directions: the limitation "directly beneath" is met because a strictly vertical line can be drawn from the select gate that intersects with the source diffusion), a bit line (horizontal portion of 40 in Figure 4b) (col. 6, l. 54) above each row, a bit line contact (vertical portion of 40) interconnecting the bit line in each row and the bit line diffusion 38 (see Figure 4b).

On claim 16: Noda teaches stacked gates and the stacked gates are self-aligned relative to each other (col. 6, l. 48-51).

On claim 17: Noda teaches including a relatively thin tunnel oxide 34 (col. 1, l. 20-35 and col. 6, l. 35-36) between the floating gates and the substrate, a first relatively thick dielectric 39 between the floating gates and the select gates, and a second relatively thick dielectric 39 between floating gates and control gates. N.B.: Attention is drawn to the appearance of a relative term, "relatively thick", and the consequent rejection under 35 U.S.C. 112, second paragraph made above. The assumption of the examiner under which the art rejection of claim 3 has been provided is that a range of thickness for both first and second "relatively thick" dielectrics that is not necessarily restricted to the regime in which tunneling can take place to an extent noticeable in the operation of the device.

On claim 18: The control gates and the select gates surround the floating gates (see Figure 4b). Referring to the rejection under 35 U.S.C., 112, second paragraph as made above, the remainder of the limitation of this claim is indefinite for containing relative terms "relatively large" and "high-voltage": some capacitance is implied by the proximity of control, floating, and select gates, and the examiner has assumed that

some capacitance meets the claim in the absence within the specification of any specific measure with which the relative terms can be viewed to acquire a definite meaning within context.

On claim 19: Noda teaches (title, abstract, Figures 3 and 4b, and col. 6, l. 26 – 62) a NAND flash memory cell array, comprising: a substrate 30 (col. 6, l. 30) having an active area 32 (col. 6, l. 30), a plurality (for the plurality see Figure 3 in which there are at least two control gate lines CGL depicted) of vertically stacked pairs of floating gates 35 and control gates 37 (see Figure 4b) arranged in rows above the active area, with the control gates being positioned above the floating gates, select gates aligned SG1, SG2,..., (col. 6, l. 46) with and positioned on both sides of each of the stacked gates (Figures 3 and 4b), a bit line (horizontal portion of 40 in Figure 4b) (col. 6, l. 54) above each row, a bit line diffusion 38 (col. 6, l. 49) in the active area toward a first end of each row (left end in Figure 4b), a bit line contact (vertical portion of 40) interconnecting the bit line in each row and the bit line diffusion 38, and a source region 38 (col. 6, l. 48-51) in the active area only partially overlapped (overlapped by virtue of being produced by a self-aligned method: see col. 6, l. 48-51, in which the lateral diffusion that inherently causes a lateral spread of the implanted ions in both directions hence inter alia in directions leading under the select gate used as mask in the self-aligned process step; the overlap is only partial because the select gate is used as a mask (loc.cit.)) by the select gate at a second end of each row (right hand side corresponding to the opposite end from the bitline contact).

On claim 20: Noda teaches stacked gates and the stacked gates are self-aligned relative to each other (col. 6, l. 48-51).

On claim 21: Noda teaches including a relatively thin tunnel oxide 34 (col. 1, l. 20-35 and col. 6, l. 35-36) between the floating gates and the substrate, a first relatively thick dielectric 39 between the floating gates and the select gates, and a second relatively thick dielectric 39 between floating gates and control gates. N.B.: Attention is drawn to the appearance of a relative term, "relatively thick", and the consequent rejection under 35 U.S.C. 112, second paragraph made above. The assumption of the examiner under which the art rejection of claim 3 has been provided is that a range of thickness for both first and second "relatively thick" dielectrics that is not necessarily restricted to the regime in which tunneling can take place to an extent noticeable in the operation of the device.

On claim 22: The control gates and the select gates surround the floating gates (see Figure 4b). Referring to the rejection under 35 U.S.C., 112, second paragraph as made above, the remainder of the limitation of this claim is indefinite for containing relative terms "relatively large" and "high-voltage": some capacitance is implied by the proximity of control, floating, and select gates, and the examiner has assumed that some capacitance meets the claim in the absence within the specification of any specific measure with which the relative terms can be viewed to acquire a definite meaning within context.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hsu et al. (6,911,690 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
July 20, 2005

Patent Examiner:

Johannes Mondt (Art Unit: 2826).